DRAFT

TURFTS Memory Map

APPROVED BY: _____

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A1 - Gateway Controller Module

ADDR	R/W	Function & Bit Pattern
$0000	W	Scope Bus Source Select Register:

b7 - NC
b6 - NC
b5 - Scope Channel-B, Address Sel bit - A2
b4 - Scope Channel-B, Address Sel bit - A1
b3 - Scope Channel-B, Address Sel bit - A0

A2	A1	A0	Function
0	0	0	Analog Monitor Bus, Demodulator I-Ch
0	0	1	Analog Monitor Bus, DSP EL-I
0	1	0	Analog Monitor Bus, DSP OT-I
0	1	1	Analog Monitor Bus, Spare_1
1	0	0	Digital Scope Bus, Ch-B
1	0	1	Analog Monitor Bus, not used
1	1	0	Analog Monitor Bus, Subcarrier RCVR I-Ch
1	1	1	Analog Monitor Bus, Spare_2

b2 - Scope Channel-A, Address Sel bit - A2
b1 - Scope Channel-A, Address Sel bit - A1
b0 - Scope Channel-A, Address Sel bit - A0

A2	A1	A0	Function
0	0	0	Analog Monitor Bus, Demodulator Q-Ch
0	0	1	Analog Monitor Bus, DSP EL-Q
0	1	0	Analog Monitor Bus, DSP OT-Q
0	1	1	Analog Monitor Bus, Spare_3
1	0	0	Digital Scope Bus, Ch-A
1	0	1	Analog Monitor Bus, PM Combiner
1	1	0	Analog Monitor Bus, Subcarrier RCVR Q-Ch
1	1	1	Analog Monitor Bus, Spare_4

A2 - Reference Frequency Source Module

ADDR	R/W	Function & Bit Pattern
$4000	R	Module ID = $4 (bits 4 thru 7) b7 - Wired to logic '0' b6 - Wired to logic '1' b5 - Wired to logic '0' b4 - Wired to logic '0' b3 ..b0 - Wired to logic '0'
$4001	R	Reference Frequency Signal Present Indicators b7..b5 - Wired to logic '0' b4 - 280 MHz Signal: OK/ERR b3 - 110 MHz Signal: OK/ERR b2 - 70 MHz Signal: OK/ERR b1 - 50 MHz Signal: OK/ERR b0 - 10 MHz Signal: OK/ERR

A3 - Transmitter Frequency Synthesizer Module

ADDR	R/W	Function & Bit Pattern
$5000	R	Module ID = $5 (bits 4 thru 7) b7 - Wired to logic '0' b6 - Wired to logic '1' b5 - Wired to logic '0' b4 - Wired to logic '1' b3..b0 - Wired to logic '0'
$5001	R	Reference Frequency Signal Present Indicators b7 - Module Status: 1=FAULT, 0=OK b6 - nc b5 - nc b4 - PN Clock Status: 1=LOCK, 0=NOT_LOCK b3 - Xlator LO Output Signal Present: 1=OK, 0=ERR b2 - Xlator Loop Status: 1=LOCK, 0=NOT_LOCK b1 - TX LO Output Signal Present: 1=OK, 0=ERR b0 - TX Synth Mixer Loop Status: 1=NOT_LOCK, 0=LOCK
$5000	W	Transmitter PN Code Generator: Control Register #1 b7 - TDRSS mode select bit-S1 b6 - TDRSS mode select bit-S0 S1 S0 TDRSS Mode 0 0 F/L 0 1 R/L Mode 1 1 0 R/L Mode 2 1 1 R/L Mode 3 b5 - Select Acq. PN Code (SPN), select bit-1 b4 - Select Acq. PN Code (SPN), select bit-0 S1 S0 SPN Code 0 0 IPN 0 1 QPN 1 0 Noise Code 1 1 No code b3 - Q-Code: ENA/INHIBIT b2 - I-Code: ENA/INHIBIT b1 - Tracking PN Code (TKPN): QPN/IPN b0 - Step Size: 1=0.5Chip/0=1023Chips
$5001	W	Transmitter PN Code Generator, Reg-A Start Vector, MSB
$5002	W	Transmitter PN Code Generator, Reg-A Start Vector, LSB
$5003	W	Transmitter PN Code Generator, Reg-C Feedback Taps, MSB
$5004	W	Transmitter PN Code Generator, Reg-C Feedback Taps, CSB
$5005	W	Transmitter PN Code Generator, Reg-C Feedback Taps, LSB
$5006	W	Transmitter PN Code Generator, Reg-C Start Vector, MSB
$5007	W	Transmitter PN Code Generator, Reg-C Start Vector, LSB
$5008	W	TX PN Code Generator, Initialize PNG, Data=xx
$5009	W	TX PN Code Generator, Clear Acq., Data=xx, Rcvr Function
$500A	W	TX PN Code Generator, Start Acq., Data=xx, Rcvr Function

A3 - Transmitter Frequency Synthesizer Module - Con't

ADDR R/W Function & Bit Pattern

$500B W Transmitter PN Code Generator: Control Register #2
- b1..7 - nc
- b0 - TX Long Code Jamset Enable: ENA/INHIBIT

$500F W TX PN Code Generator, PN Step, Data=xx, Rcvr Function

$5010 W Monitor Bus: Channel Select Register
- b7 - Scope Sync Select Bit-1
- b6 - Scope Sync Select Bit-0

b7	b6	Function
0	0	TX Short Code Epoch
0	1	TX Long Code Epoch
1	0	TX PN Code Clock
1	1	not used

- b5..b3 - n/c
- b2 - Scope Channel-A Select Bit-2
- b1 - Scope Channel-A Select Bit-1
- b0 - Scope Channel-A Select Bit-0

b2	b1	b0	FUNCTION
0	0	0	TX I-PN Code
0	0	1	TX Q-PN Code
0	1	0	TX PN Code Clock
0	1	1	TX Long Code Epoch
1	0	0	TX Short Code Epoch
1	0	1	TX PNG X4-Clock
1	1`	0	Set to logic '0'
1	1	1	Set to logic '0'

$5011 W Monitor Bus: Module Enable Register
- b7 thru b3 - n/c
- b2 - Scope Sync: /ENA
- b1 - n/c
- b0 - Scope Channel-A: /ENA

($5400..$57FF RW TX Freq Synth Controller Dual-Port RAM, 1K Bytes)
-First table entry:
$5400..3Table Freq Offset, NCO Control Word, ms-word 4-bytes (48-bit CW)
$5404..5Table Freq Offset, NCO Control Word, ls-word 2-bytes.
$5406..9Table Freq Offset, NCO Control Word, ls-word 2-bytes (32-bit CW)
-Second table entry:
$540a..dTable Freq Offset, NCO Control Word, ms-word 4-bytes. (48-bit CW)
$540e..f Table Freq Offset, NCO Control Word, ls-word 2-bytes.
$5410..3Table Freq Offset, NCO Control Word, ls-word 2-bytes. (32-bit CW)
|
| (total of 98 table entries)
|
-98th table entry:

A3 - Transmitter Frequency Synthesizer Module - Con't

ADDR R/W Function & Bit Pattern
$57ca..d Table Freq Offset, NCO Control Word, ms-word, 4-bytes. (48-bit CW)
$57ce..f Table Freq Offset, NCO Control Word, ls-word, 2-bytes.
$57d0..3 Table Freq Increment, NCO Control Word, 4-bytes.

-Status Block:
$57de..1 Current Freq Status, NCO Control Word, ms-word, 4-bytes (total of 48-bits)
$57e2..3 Current Freq Status, NCO Control Word, ls-word, 2-bytes
$57e4..7 Time tic, 250 microsecond, repeats every 298 hours, 4-bytes
$57e8 Table Index, Ranges from 0 to 97.
$57e9 Sweep Status:
- b7 - spare
- b6 - Wait for TONS Sync: 1=WAITING 0=SYNC
- b5..4 - Sweep Status:
  - 0 - Running
  - 1 - Holding
  - 2 - Slew-to-Zero
- b3..0 - Sweep Mode:
  - 0 - Sweep Off
  - 1 - Continuous
  - 2 - One_Way
  - 3 - Table Sweep - Wait for Sync
  - 4 - Table Sweep - w/o Wait for Sync

-Control Block:
$57ea..b Freq Dwell, (Number of 250 microseconds to stop at the frequency extremes), 2-bytes
$57ec..f Center Frequency, NCO Control Word, ms-word, 4-bytes (total of 48-bits)
$57f0..1 Center Frequency, NCO Control Word, ls-word, 2-bytes
$57f2..5 Frequency Range, NCO Control Word, ms-word, 4-bytes (total of 48-bits)
$57f6..7 Frequency Range, NCO Control Word, ls-word, 2-bytes
$57f8..b Frequency Increment, NCO Control Word, ms-word, 4-bytes (total of 48-bits)
$57fc..d Frequency Increment, NCO Control Word, ls-word, 2-bytes
$57fe Spare Byte
$57ff Command Byte:
- 1 - Set Single Frequency Mode
- 2 - Set Continuous Sweep Mode
- 3 - Set One-Way Sweep Mode
- 4 - Set Table Sweep Mode, Wait-for-Sync
- 5 - Set Table Sweep Mode, don’t wait for sync.
- 6 - Jump-to-Zero Command
- 7 - Slew-to-Zero Command
- 8 - Hold Command
- 10 - Release Hold Command

A4 - Receiver Frequency Synthesizer Module

ADDR R/W Function & Bit Pattern

$6000 R Module ID = $6 (bits 4 thru 7)
- b7 - Wired to logic '0'
- b6 - Wired to logic '1'
- b5 - Wired to logic '1'
- b4 - Wired to logic '0'
- b3 - Fault Monitor: 1=OK/0=ERR
- b2 - RX LO Signal Present: 1=OK/0=ERR
- b1 - Carrier Loop LO Signal Present: 1=OK/0=ERR
- b0 - RX Mixer Loop Lock: 1=LOCK/0=UNLOCK

$6000 W Monitor Bus: Channel Select Register
- b7 - Scope Sync Select Bit-1
- b6 - Scope Sync Select Bit-0

Monitor Bus: Scope Sync

b7	b6	Function
0	0	RX Short Code Epoch
0	1	RX Long Code Epoch
1	0	Dither Clock
1	1	not used

- b5 - Scope Channel-B Select Bit-2
- b4 - Scope Channel-B Select Bit-1
- b3 - Scope Channel-B Select Bit-0

Monitor Bus: Channel-B

b2	b1	b0	Function
0	0	0	RX I-PN Code
0	0	1	RX Q-PN Code
0	1	0	RX SPN Code
0	1	1	RX TKPN Code
1	0	0	RX Short Code Epoch
1	0	1	RX Long Code Epoch
1	1	0	Sync (to TX Epoch) Complete
1	1	1	Dither Clock

- b2 - n/c
- b1 - n/c
- b0 - n/c

$6001 W Monitor Bus: Module Enable Register
- b7..b3 - n/c
- b2 - Scope Sync: /ENA
- b1 - Scope Channel-B: /ENA
- b0 - n/c

A4 - Receiver Frequency Synthesizer Module - Con't

ADDR R/W Function & Bit Pattern

DSP_Bus

ADDR R/W Function & Bit Pattern

$40 W PN Code Generator: Command Register

b7 - TDRSS mode select bit-S1

b6 - TDRSS mode select bit-S0

S1	S0	TDRSS Mode
0	0	F/L
0	1	R/L Mode 1
1	0	R/L Mode 2
1	1	R/L Mode 3

b5 - Select Acq. PN Code (SPN), select bit-1

b4 - Select Acq. PN Code (SPN), select bit-0

S1	S0	SPN Code
0	0	IPN
0	1	QPN
1	0	Noise Code
1	1	No code

b3 - Q-Code: ENA/INHIBIT

b2 - I-Code: ENA/INHIBIT

b1 - Tracking PN Code (TKPN): QPN/IPN

b0 - Step Size: 1=0.5Chip/0=1023Chips

$41 W PN Code Generator, Reg-A Start Vector, MSB
$42 W PN Code Generator, Reg-A Start Vector, LSB
$43 W PN Code Generator, Reg-C Feedback Taps, MSB
$44 W PN Code Generator, Reg-C Feedback Taps, CSB
$45 W PN Code Generator, Reg-C Feedback Taps, LSB
$46 W PN Code Generator, Reg-C Start Vector, MSB
$47 W PN Code Generator, Reg-C Start Vector, LSB
$48 W PN Code Generator, Initialize PNG, Data=xx
$49 W PN Code Generator, Clear Acq., Data=xx, Rcvr Function
$4A W PN Code Generator, Start Acq., Data=xx, Rcvr Function
$4B W Transmitter PN Code Generator: Control Register #2

b1..7 - nc

b0 - TX Long Code Jamset Enable: ENA/INHIBIT

$4F W PN Code Generator, PN Step, Data=xx, Rcvr Function

A4 - Receiver Frequency Synthesizer Module - Con't

DSP_Bus

ADDR R/W Function & Bit Pattern

Rx Carrier Freq Source (Qualcomm Q2334 Dual DDS), DDS #1:

$00	W	Phase Increment A (PIRA) 1, bits 0-7 (LSB)
01	W	" " , bits 8-15
02	W	" " , bits 16-23
03	W	" " , bits 24-31 (MSB)
04	W	Phase Increment B (PIRB) 1, bits 0-7 (LSB)
05	W	" " , bits 8-15
06	W	" " , bits 16-23
07	W	" " , bits 24-31 (MSB)
08	W	Synchronous Mode Control (SMC) 1 b7..4 - xxx b3 - Hop Clock PM Mod Enable (HPME) b2 - External Mux Enable (EME) b1 - External PM Mod Enable (EPME) b0 - xxx
09	W	Reserved
0A	W	Asynchronous Mode Control (AMC) 1 b7..6 - xxx b5 - PM Register Add Enable (PMAE) b4 - xxx b3 - Output Format: 0=2's compl, 1=offset binary b2..0 - D/A converter Size: set to 0x06, 12 bits
0B	W	Reserved
0C	W	Accumulator Reset (ARR) 1
0D	W	Reserved
0E	W	Asynchronous Hop Clock (AHC) 1
0F	W	Reserved

(Spare NCO) (Qualcomm Q2334 Dual DDS), DDS #2:

$10	W	Phase Increment A (PIRA) 2, bits 0-7 (LSB)
11	W	" " , bits 8-15
12	W	" " , bits 16-23
13	W	" " , bits 24-31 (MSB)
14	W	Phase Increment B (PIRB) 2, bits 0-7 (LSB)
15	W	" " , bits 8-15
16	W	" " , bits 16-23
17	W	" " , bits 24-31 (MSB)
18	W	Synchronous Mode Control (SMC) 2
19	W	Reserved
1A	W	Asynchronous Mode Control (AMC) 2
1B	W	Reserved
1C	W	Accumulator Reset (ARR) 2
1D	W	Reserved
1E	W	Asynchronous Hop Clock (AHC) 2
1F	W	Reserved

A4 - Receiver Frequency Synthesizer Module - Con't

DSP Bus

ADDR	R/W	Function & Bit Pattern
		Carr Loop Freq Source (Qualcomm Q2334 Dual DDS), DDS #1:
$20	W	Phase Increment A (PIRA) 1, bits 0-7 (LSB)
21	W	" " , bits 8-15
22	W	" " , bits 16-23
23	W	" " , bits 24-31 (MSB)
24	W	Phase Increment B (PIRB) 1, bits 0-7 (LSB)
25	W	" " , bits 8-15
26	W	" " , bits 16-23
27	W	" " , bits 24-31 (MSB)
28	W	Synchronous Mode Control (SMC) 1
29	W	Reserved
2A	W	Asynchronous Mode Control (AMC) 1
2B	W	Reserved
2C	W	Accumulator Reset (ARR) 1
2D	W	Reserved
2E	W	Asynchronous Hop Clock (AHC) 1
2F	W	Reserved
		PN Loop Freq Source (Qualcomm Q2334 Dual DDS), DDS #2:
$30	W	Phase Increment A (PIRA) 2, bits 0-7 (LSB)
31	W	" " , bits 8-15
32	W	" " , bits 16-23
33	W	" " , bits 24-31 (MSB)
34	W	Phase Increment B (PIRB) 2, bits 0-7 (LSB)
35	W	" " , bits 8-15
36	W	" " , bits 16-23
37	W	" " , bits 24-31 (MSB)
38	W	Synchronous Mode Control (SMC) 2
39	W	Reserved
3A	W	Asynchronous Mode Control (AMC) 2
3B	W	Reserved
3C	W	Accumulator Reset (ARR) 2
3D	W	Reserved
3E	W	Asynchronous Hop Clock (AHC) 2
3F	W	Reserved

A5 - Receiver IF Tracking Module

ADDR R/W Function & Bit Pattern

$8000 R Module ID = $8 & Status Register (bits 4 thru 7)
- b7 - Wired to logic '1'
- b6 - Wired to logic '0'
- b5 - Wired to logic '0'
- b4 - Wired to logic '0'
- b3 - Carrier Loop LO Signal Detect: OK/FAULT
- b2 - PN Loop LO Signal Detect: OK/FAULT
- b1 - TKPN LO Signal Detect: OK/FAULT
- b0 - SPN LO Signal Detect: OK/FAULT

$8001 R LO Signal Status
- b1 - LO Fault
- b0 - 370 MHz IF Overload

$8000 W RF Monitor Control Register. (A5-RF Monitor to RFD-EXT SPA IN)
- b7..b2 - not used
- b1 - Switch Control: SC1
- b0 - Switch Control: SC0

SC1	SC0	Switch Control Logic
0	0	370 MHz IF
0	1	External RF In from A5J2
1	0	PN Loop 70 MHz IF
1	1	Carrier Loop 70 MHz IF

DSP_Bus

ADDR R/W Function & Bit Pattern

$50 W Rx 370 MHz IF Gain Control (0 thru 63.5 dB Atten)
- b7 - Receiver Lock: 1=LOCK 0=UNLOCKED
- b6 - 32 dB Section
- b5 - 16 dB
- b4 - 8 dB
- b3 - 4 dB
- b2 - 2 dB
- b1 - 1 dB
- b0 - 0.5 dB

A6 - Receiver Data Demodulator Module

ADDR R/W Function & Bit Pattern

$9000 R Module ID = $9 (bits 4 thru 7)
- b7 - Wired to logic '1'
- b6 - Wired to logic '0'
- b5 - Wired to logic '0'
- b4 - Wired to logic '1'
- b3 - Q-Ch Demod LO Sig Det: OK/FAULT
- b2 - I-Ch Demod LO Sig Det: OK/FAULT
- b1 - Q-PN LO Sig Det: OK/FAULT
- b0 - I-PN LO Sig Det: OK/FAULT

$9000 W I-Channel Control Regester-A
- b7 - IF Monitor Source Select: Q-CH/I-CH
- b6 - IF Bandwidth Select: NB/WB
- b5 - PD Filter BW Select, S1
- b4 - PD Filter BW Select, S0

S1	S0	Function
0	0	Switchable Low Pass Filter(SLPF)
0	1	600 KHz LP Filter
1	0	10 MHz LP Filter
1	1	Inhibit Output (Turn it off!)

- b3 - SLPF Control bit DN-800: ENA/OUT
- b2 - SLPF Control bit DN-400: ENA/OUT
- b1 - SLPF Control bit DN-200: ENA/OUT
- b0 - SLPF Control bit DN-100: ENA/OUT

$9001 W I-Channel Control Regester-B
- b7 - SLPF Control bit DN-80 : ENA/OUT
- b6 - SLPF Control bit DN-40 : ENA/OUT
- b5 - SLPF Control bit DN-20 : ENA/OUT
- b4 - SLPF Control bit DN-10 : ENA/OUT
- b3 - SLPF Control bit DN-8 : ENA/OUT
- b2 - SLPF Control bit DN-4 : ENA/OUT
- b1 - SLPF Control bit DN-2 : ENA/OUT
- b0 - SLPF Control bit DN-1 : ENA/OUT

A6 - Receiver Data Demodulator Module - Cont'd

ADDR	R/W	Function & Bit Pattern
$9002	W	Q-Channel Control Regester-A

b7 -
b6 - IF Bandwidth Select: NB/WB
b5 - PD Filter BW Select, S1
b4 - PD Filter BW Select, S0

S1	S0	Function
0	0	Switchable Low Pass Filter(SLPF)
0	1	600 KHz LP Filter
1	0	6 MHz LP Filter
1	1	Inhibit Output (Turn it off!)

b3 - SLPF Control bit DN-800: ENA/OUT
b2 - SLPF Control bit DN-400: ENA/OUT
b1 - SLPF Control bit DN-200: ENA/OUT
b0 - SLPF Control bit DN-100: ENA/OUT

$9003 W Q-Channel Control Regester-B

b7 - SLPF Control bit DN-80 : ENA/OUT
b6 - SLPF Control bit DN-40 : ENA/OUT
b5 - SLPF Control bit DN-20 : ENA/OUT
b4 - SLPF Control bit DN-10 : ENA/OUT
b3 - SLPF Control bit DN-8 : ENA/OUT
b2 - SLPF Control bit DN-4 : ENA/OUT
b1 - SLPF Control bit DN-2 : ENA/OUT
b0 - SLPF Control bit DN-1 : ENA/OUT

A6 - Receiver Data Demodulator Module - Cont'd

ADDR R/W Function & Bit Pattern

Switchable Low Pass Filter (Datel FLJ-D2) logic coding table:

Fc	SLPF Control bit to be Enabled
100 Hz	DN-1
200 Hz	DN-2
400 Hz	DN-4
800 Hz	DN-8
1 KHz	DN-10
2 KHz	DN-20
4 KHz	DN-40
8 KHz	DN-80
10 KHz	DN-100
20 KHz	DN-200
40 KHz	DN-400
80 Khz	DN-800
90 KHz	DN-800, DN-100
100 KHz	DN-800, DN-200
120 KHz	DN-800, DN-400
140 KHz	DN-800, DN-400, DN-200
150 KHz	DN-800, DN-400, DN-200, DN-100
159.9KHz	DN-800, DN-400, DN-200, DN-100, DN-80

$9004,5 W I-Channel 70 MHz Reference Phase Adjust DAC buffer.

Write a 16-bit word to the DAC input buffer. The DAC outputs a Voltage proportional to the digital word, 0 thru 10 Volts. The Update Strobe is issued on the LS-Byte write cycle. Both I-Ch & Q-Ch input buffers are transfered to the respective DAC's.

$9006,7 W Q-Channel 70 MHz Reference Phase Adjust DAC buffer.

Write a 16-bit word to the DAC input buffer. The DAC outputs a Voltage proportional to the digital word, 0 thru 10 Volts. The Update Strobe is issued on the LS-Byte write cycle. Both I-Ch & Q-Ch input buffers are transfered to the respective DAC's.

$9009 W Demod I/Q Ratio Select Register

b5 - Q Ch Attenuator: 4dB/0dB
b4 - Q Ch Attenuator: 2dB/0dB
b3 - Q Ch Attenuator: 1dB/0dB
b2 - I Ch Attenuator: 4dB/0dB
b1 - I Ch Attenuator: 2dB/0dB
b0 - I Ch Attenuator: 1dB/0dB

A7 - Digital Signal Processor (DSP) Module

ADDR	R/W	Function & Bit Pattern
$33000	R	Module ID = $7 (bits 4 thru 7) (TSPU Addr = $7000)
		b7 - Set to logic '0'
		b6 - Set to logic '1'
		b5 - Set to logic '1'
		b4 - Set to logic '1'
		b3..b0 - Set to logic '0'
$33001..3	R	NOT USED - READ AS '0'
$33004	R	DSP Present: PRESENT (FFh)/NOT PRESENT (00h)
$33005..7	R	NOT USED - READ AS '0'
$33008	R/W	DPRAM Occupied: OCCUPIED (FFh)/UNOCCUPIED (00h)
$33009..B	R	NOT USED - READ AS '0'
$3300C..F	R	Data Tag
$33010	R	Receiver Status
		b7 - DSP Board Status: READY/NOT READY
		b6 - Frequency Sweep Status: ON/OFF OR HELD
		b5 - Carrier Lock Status: LOCKED/UNLOCKED
		b4 - PN Code Lock Status: LOCKED/UNLOCKED
		b3 - NOT USED
		b2 - DSP State b2
		b1 - DSP State b1
		b0 - DSP State b0
$33011	R	Error Message - TBD
$33012..3	R	NOT USED - READ AS '0'
$33014..7	R	Lowpass Filter Bandwidth *
$33018	R	DCA Control Word
$33019..B	R	NOT USED - READ AS '0'
$3301C..F	R	PN Correlation *
$33020..3	R	Data Rate *
$33024..7	R	Signal Loss *
$33028..B	R	PN Code Phase Error *
$3302C..F	R	PN NCO Control Word
$33030..3	R	Carrier Lock Measurement *
$33034..7	R	Receiver Mode:
		b7 - PN Code Function: INH/ENA
		b6..b2 - not used
		b1 - TDRSS Mode B1
		b0 - " " B0

B1	B0	Mode
0	0	F/L
0	1	R/L Mode-1
1	0	R/L Mode-2
1	1	R/L Mode-3

A7 - Digital Signal Processor (DSP) Module - Cont'd

ADDR	R/W	Function & Bit Pattern
$33038..B	R	PNGEN Command Byte
		b7..3 - n/u
		b2 - S. ACQ Enable/Disable
		b1 - TKPN Select Q/I
		b0 - SPN Select Q/I
$33039..B	R	NOT USED - READ AS '0'
$3303C..F	R	Carrier NCO Control Word
$33040..3	R	Sweep Rate *
$33044..7	R	Sweep Range *
$33048..B	R	RX NCO Control Word
$3304C..F	R	TX NCO Control Word
$33050..3	R	Carrier Loop Phase Error *
$33054..$33FB7	NOT USED - READ AS '0'	
$33FB8	W	Input Signal Parameters
		b7 - PN Codes: DISABLE/ENABLE
		b6 - Lowpass Filter BW Select: MANUAL/AUTO
		b5 - I:Q Ratio Select Bit-2
		b4 - I:Q Ratio Select Bit-1
		b3 - I:Q Ratio Select Bit-0
		I:Q Ratio Select
		b5 b4 b3 I:Q Ratio
		0 0 0 1:1
		0 0 1 1:2
		0 1 0 1:4
		0 1 1 4:1
		1 0 0 10:1
		b2 - Data Type Select: BIPHASE/NRZ
		b1 - TDRSS Mode Select Bit-1
		b0 - TDRSS Mode Select Bit-0
		TDRSS Mode Select
		b1 b0 TDRSS Mode
		0 0 F/L
		0 1 R/L DG 1 Mode 1
		1 0 R/L DG 1 Mode 2
		1 1 R/L DG 1 Mode 3
$33FB9..B	W	NOT USED - WRITE '0'
$33FBC..F	W	Data Rate *

A7 - Digital Signal Processor (DSP) Module - Cont'd

ADDR	R/W	Function & Bit Pattern
$33FC0..3	W	Lowpass Filter Bandwidth *(If $33FB8-b6 is '1')
$33FC4..7	W	Input Power Level *
$33FC8..B	W	NOT USED
$33FCC	W	PNGEN Status Byte: b7..b3 - n/c b2 - S. ACQ Enable/Disable b1 - TKPN Selected Q/I b0 - SPN Selected Q/I
$33FCD..DB	W	NOT USED - WRITE '0'
$33FDC	W	Frequency Sythesizer Command b7..b5 - n/c b4 - Sweep Mode: 1-Way/2-Way b3 - Turnaround Mode Select b1 b2 - Turnaround Mode Select b0 b1 - Frequency Sweep Hold: b1 b0 - Frequency Sweep Start: b0 **Turnaround Mode** b3 b2 Turnaround Mode 0 0 Noncoherent - RX & TX Frequency Valid 0 1 Coherent - RX Frequency Valid Only 1 0 Coherent - TX Frequency Valid Only
$33FDD..F	W	NOT USED - WRITE '0'
$33FE0..3	W	Receiver Center Frequency *
$33FE4..7	W	Transmitter Center Frequency *
$33FE8..B	W	Sweep Rate *
$33FEC..F	W	Sweep Range *
$33FF0	W	Manual AGC Control Word
$33FF1..E	W	NOT USED - WRITE '0'
$33FFF	W	Control Message b7 - Reset DSP Board: RESET/NOT RESET b6 - Reacquire PN Select: REACQUIRE/NOT REAQ. b5 - Reacquire Carrier Select: REACQ./NOT REAQ b4 - Freq. Synth. Change: CHANGE/NO CHANGE b3 - Carrier Loop Change: CHANGE/NO CHANGE b2 - PN Loop Change: CHANGE/NO CHANGE b1 - Input Signal Change: CHANGE/NO CHANGE b0 - Set to '1'
$33FFF	R	DSP Read Done: = 00h if DONE, != 00h if NOT DONE

NOTE:

1. Byte 0 is the least significant byte.
2. (*) - Indicates a floating point value.

A8 - Bit-Sync & Viterbi Decoder Module

ADDR R/W Function & Bit Pattern

$2000 R Module ID = $2 (bits 4 thru 7)
- b7 - Wired to logic '0'
- b6 - Wired to logic '0'
- b5 - Wired to logic '1'
- b4 - Wired to logic '0'
- b3 - I-Ch BER Done
- b2 - I-Ch Decoder Status: 1=LOCK 0=ERROR
- b1 - Q-Ch BER Done
- b0 - Q-Ch Decoder Status: 1=LOCK 0=ERROR

$2000 W Monitor Bus: Channel Select Register
- b7 - n/c
- b6 - n/c
- b5 - Scope Channel-B Select:
  - 0 - Q-Ch Differential Decoded Data Output
  - 1 - Q-Ch Differential Decoded Data Clock Output
  - 2 - Q-Ch Symbol Output
  - 3 - Q-Ch Conv Decoded Data Output
  - 4 - Q-Ch Symbol Clock Output
  - 5 - Q-Ch Conv Decoded Data Clock Output
  - 6 - Set to logic '0'
  - 7 - Set to logic '0'
- b2 - Scope Channel-A Select:
  - 0 - I-Ch Differential Decoded Data Output
  - 1 - I-Ch Differential Decoded Data Clock Output
  - 2 - I-Ch Symbol Clock Output
  - 3 - I-Ch Symbol Output
  - 4 - I-Ch Conv Decoded Data Output
  - 5 - I-Ch Conv Decoded Data Clock Output
  - 6 - Set to logic '0'
  - 7 - Set to logic '0'

$2001 W Monitor Bus: Module Enable Register
- b7..b2 - n/c
- b1 - Scope Channel-B: /ENA
- b0 - Scope Channel-A: /ENA

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

ADDR R/W Function & Bit Pattern

$2002 W Module Control Register
- b7 - n/c
- b6 - Q-Ch Bit-Sync Source Select: 1=Q-Ch_DEMOD 0=GN-S/C
- b5 - n/c
- b4 - I-Ch Bit-Sync Source Select: 1=I-Ch_DEMOD 0=TLM_RT
- b3 - Q-Ch Bit-Sync Source Select: 1=(depends on b6) 0=TLM_DIAG
- b2 - DeInterleaver Source select: 1=TEST 0=NORMAL
- b1 - I-Ch Bit-Sync Clock Enable Select: 1=ENABLE 0=RESET
- b0 - I-Ch Bit-Sync Clock Enable Select: 1=ENABLE 0=RESET

$2003 W I&Q-Channel Bit-Sync Reset: Data = XX

$2004 W PRESTO x8 Clock Source Frequency Select Register (Latch - 1)
- b7..b4 - Q Channel Clock divider, b7 - msb
- b3..b0 - I Channel Clock divider, b3 - msb

$2005 W I-Ch Control Register (Latch - 2)
- b7 - I-Ch Viterbi Decoder Source: 1=EXT 0=I-CH_BS
- b6 - I-Ch Bi-∅ NRZ Converter Output Select - S1
- b5 - I-Ch Bi-∅ NRZ Converter Output Select - S0

S1	S0	Function
0	0	Bi-∅-M
0	1	NRZ-L
1	0	Bi-∅-S
1	1	Bi-∅-L

- b4 - n/c
- b3 - I-Ch Symbol-2 Invert: 1=INVERT 0=NORM
- b2 - I-Ch Output Source Select: 1=BS 0=DECODER
- b1 - I-Ch Differential Decoder: 1=ENABLE 0=INHIBIT
- b0 - I-Ch Differential Decoder Input Format: 1=NRZ-S 0=NRZ-M

$2003 W Q-Ch Control Register (Latch - 3)
- b7 - Q-Ch Viterbi Decoder Source: 1=EXT 0=I-CH_BS
- b6 - Q-Ch Bi-∅ NRZ Converter Output Select - S1
- b5 - Q-Ch Bi-∅ NRZ Converter Output Select - S0

S1	S0	Function
0	0	Bi-∅-M
0	1	NRZ-L
1	0	Bi-∅-S
1	1	Bi-∅-L

- b4 - n/c
- b3 - Q-Ch Symbol-2 Invert: 1=INVERT 0=NORM
- b2 - Q-Ch Output Source Select: 1=BS 0=DECODER
- b1 - Q-Ch Differential Decoder: 1=ENABLE 0=INHIBIT
- b0 - Q-Ch Differential Decoder Input Format: 1=NRZ-S 0=NRZ-M

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2007 W I/Q Control Register (Latch - 4)

b7 - Test Only! Invert Bit-Sync MSB output: 1=INV 0=NONINV
b6 - Deinterleaver Decision Mode: 1=HARD 0=SOFT
b5 - RCVR Squelch Control, I&Q Ch, Decoder Indicator: 1=ENABLED 0=DISABLED
b4 - Q-Ch Decoder Rate: 1=THIRD 0=HALF
b3 - Q-Ch Data&Clock Output Polarity: 1=NORM 0=INV
b2 - I-Ch Data&Clock Output Polarity: 1=NORM 0=INV
b1 - PRESTO Q-Ch Divider Override: 1=DIV_BY_N 0=DIV_BY_1
b0 - PRESTO I-Ch Divider Override: 1=DIV_BY_N 0=DIV_BY_1

I-Channel Bit-Sync: STEL-2110A Read-Only Registers. 32-bytes.

$2020 R Signal Input Register. 8-bit data word of the digitized information channel input. This format is "Offset 2's Complement".

$2034 R Signal Level Reg. 2-bytes. Lock Status:
The 16 bits of the signal amplitude accumulator are presented in these two bytes. Bit-7 in address $2034 is the MS-bit and Bit-0 in address $2035 is the LS-bit.

STEL-2110A Write-Only Registers. 32-bytes.

$2030 W Timing Control Register. 1-byte. Reset Value $01.

b7 - Pre-Accumulation Control Factor, Ai, MS-bit
b6 - Pre-Accumulation Control Factor, Ai
b5 - Pre-Accumulation Control Factor, Ai, LS-bit

Ai	B7	B6	B5
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0

b4 - NCO Clock Prescale Factor, Cs, MS-bit
b3 - NCO Clock Prescale Factor, Cs
b2 - NCO Clock Prescale Factor, Cs, LS-bit

Cs	B4	B3	B2
1	0	0	0
4	0	0	1
16	0	1	0
64	0	1	1
256	1	0	0
1024	1	0	1
4096	1	1	0
16384	1	1	1

b1 - I/Q Channel Accumulator control:
b1 = 1, sets Pa = 4
b1 = 0, sets Pa = 1*

b0 - Samples per Symbol, Ss:
b0 = 1, Ss = 8*
b0 = 0, Ss = 4

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2031 W Loop Gain Control Register. 1-byte.

b7 - Gain Control Factor - K2, MS-bit
b6 - Gain Control Factor - K2
b5 - Gain Control Factor - K2
b4 - Gain Control Factor - K2, LS-bit

K2	B7	B6	B5	B4
2^{-4}	0	0	0	0
2^{-3}	0	0	0	1
2^{-2}	0	0	1	0
2^{-1}	0	0	1	1
2^{0}	0	1	0	0
2^{1}	0	1	0	1
2^{2}	0	1	1	0
2^{3}	0	1	1	1
2^{4}	1	0	0	0
2^{5}	1	0	0	1
2^{6}	1	0	1	0
2^{7}	1	0	1	1
2^{8}	1	1	0	0
2^{9}	1	1	0	1

STEL-2110A Write-Only Registers. 32-bytes.

$2031 W Loop Gain Control Register. 1-byte. - Cont'd

K2	B7	B6	B5	B4
2^{10}	1	1	1	0
2^{11}	1	1	1	1

b3 - Gain Control Factor - K1, MS-bit
b2 - Gain Control Factor - K1
b1 - Gain Control Factor - K1
b0 - Gain Control Factor - K1, LS-bit

K1	B3	B2	B1	B0
2^{0}	0	0	0	0
2^{1}	0	0	0	1
2^{2}	0	0	1	0
2^{3}	0	0	1	1
2^{4}	0	1	0	0
2^{5}	0	1	0	1
2^{6}	0	1	1	0
2^{7}	0	1	1	1
2^{8}	1	0	0	0
2^{9}	1	0	0	1
2^{10}	1	0	1	0
2^{11}	1	0	1	1
2^{12}	1	1	0	0
2^{13}	1	1	0	1
2^{14}	1	1	1	0
2^{15}	1	1	1	1

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2032 W Bit Rate Control Register. 3-bytes.

These three bytes control the MS-bits of the 27-bit NCO's Phase Register. Bit-7 of address $2032 is the MS-bit and bit-0 of $2024 is the LSB.

$2037 W Mode Control Register. 1-byte. Reset Value: $81.

b7 - Software Reset, 0 = Reset.
b6 - Loop Offset Control, MS-bit.
b5 - Loop Offset Control
b4 - Loop Offset Control, LS-bit.

Offset	B6	B5	B4
-3/4	1	1	1
-1/2	1	1	0
-1/4	1	0	1
0	X	0	0 (default)
+1/4	0	0	1
+1/2	0	1	0
+3/4	0	1	1

b3 - Freeze Data Control.
b2 - Coherent DPSK Enable Control:
Set to 0, default.
Set to 1, disables Q arm of dot product generator.
b1 - Loop Filter Input Control:
Set to 0, bit timming discriminator is connected to the loop filter (default).
Set to 1, FBI_{8-0} inputs are connected.
b0 - Input Data Format Control:
Set to 0, I_{s5-0} and Q_{s5-0} inputs are two's offset complement.
Set to 1, is offset binary format.

I-Channel Convolutional Decoder:
Qualcomm Q1650 Read-Only registers. 32-bytes.

$2043 R BER Measurement LS-Byte Output Register.
$2044 R BER Measurement MS-Byte Output Register.

$2042 W Decoder Control Register #1.

b7..b5 - 0
b4 - Rate 1/3 Decoder Enable: 1=ENABLE 0=INHIBIT
b3 - 0
b2 - Rate 1/2 decoder enable: : 1=ENABLE 0=INHIBIT
b1 - 0
b0 - Input Mode: 1=SERIAL 0=PARALLEL

$2043 W Decoder Control Register #2.

b7..b5 - 0
b4 - Differential Decoder Enable: 1=ENABLE 0=DISABLE
b3 - Direct Data Mode: 1=BUS 0=PINS
b2 - 0
b1 - 0
b0 - Decoder Input Mode: 1=SIGN_MAG 0=OFFSET_BINARY

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2044 W Decoder Control Register #3.
b7..b3 - 0
b2 - S/W Decoder Reset: 1=RESET 0=RUN
b1 - 0
b0 - ChainBack Path Depth: 1=96_STATES 0=/48_STATES

$2048 W Normalization Test Bit Count Input Register.
(Determines the length of the synchronization monitor test)

$2049 W Normalization Test Normalize Count Input Register.
(Determines the normalization threshold level for the synchronization monitor test)

$204A W BER Period Input Register LS-Byte of 24-bit value.
$204B W BER Period Input Register CS-Byte
$204C W BER Period Input Register MS-Byte

$2055 W Reserved Register. Set to '0'. Must Write '0'
$2056 W Reserved Register. Set to '0'. Must Write '0'
$2057 W Normalization Test Value Enable Register.
Value is a Don't Care. Restarts the test.

$2058 W BER Test Value Enable Register.
Value is a Don't Care. Restarts the test.

Q-Channel Bit-Sync:
STEL-2110A Read-Only Registers. 32-bytes.

$2060 R Signal Input Register. 8-bit data word of the digitized information channel input. This format is "Offset 2's Complement".

$2074 R Signal Level Reg. 2-bytes. Lock Status:
The 16 bits of the signal amplitude accumulator are presented in these two bytes. Bit-7 in address $2034 is the MS-bit and Bit-0 in address $2035 is the LS-bit.

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2070 W Timing Control Register. 1-byte. Reset Value $01.

b7 - Pre-Accumulation Control Factor, Ai, MS-bit
b6 - Pre-Accumulation Control Factor, Ai
b5 - Pre-Accumulation Control Factor, Ai, LS-bit

Ai	B7	B6	B5
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0

b4 - NCO Clock Prescale Factor, Cs, MS-bit
b3 - NCO Clock Prescale Factor, Cs
b2 - NCO Clock Prescale Factor, Cs, LS-bit

Cs	B4	B3	B2
1	0	0	0
4	0	0	1
16	0	1	0
64	0	1	1
256	1	0	0
1024	1	0	1
4096	1	1	0
16384	1	1	1

b1 - I/Q Channel Accumulator control:
b1 = 1, sets Pa = 4
b1 = 0, sets Pa = 1*

b0 - Samples per Symbol, Ss:
b0 = 1, Ss = 8*
b0 = 0, Ss = 4

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2071 W Loop Gain Control Register. 1-byte.

b7 - Gain Control Factor - K2, MS-bit
b6 - Gain Control Factor - K2
b5 - Gain Control Factor - K2
b4 - Gain Control Factor - K2, LS-bit

K2	B7	B6	B5	B4
2^{-4}	0	0	0	0
2^{-3}	0	0	0	1
2^{-2}	0	0	1	0
2^{-1}	0	0	1	1
2^{0}	0	1	0	0
2^{1}	0	1	0	1
2^{2}	0	1	1	0
2^{3}	0	1	1	1
2^{4}	1	0	0	0
2^{5}	1	0	0	1
2^{6}	1	0	1	0
2^{7}	1	0	1	1
2^{8}	1	1	0	0
2^{9}	1	1	0	1
2^{10}	1	1	1	0
2^{11}	1	1	1	1

b3 - Gain Control Factor - K1, MS-bit
b2 - Gain Control Factor - K1
b1 - Gain Control Factor - K1
b0 - Gain Control Factor - K1, LS-bit

K1	B3	B2	B1	B0
2^{0}	0	0	0	0
2^{1}	0	0	0	1
2^{2}	0	0	1	0
2^{3}	0	0	1	1
2^{4}	0	1	0	0
2^{5}	0	1	0	1
2^{6}	0	1	1	0
2^{7}	0	1	1	1
2^{8}	1	0	0	0
2^{9}	1	0	0	1
2^{10}	1	0	1	0
2^{11}	1	0	1	1
2^{12}	1	1	0	0
2^{13}	1	1	0	1
2^{14}	1	1	1	0
2^{15}	1	1	1	1

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2072 W Bit Rate Control Register. 3-bytes.

These three bytes control the MS-bits of the 27-bit NCO's Phase Register. Bit-7 of address $2072 is the MS-bit and bit-0 of $2074 is the LSB.

$2077 W Mode Control Register. 1-byte. Reset Value: $81.

b7 - Software Reset, 0 = Reset.
b6 - Loop Offset Control, MS-bit.
b5 - Loop Offset Control
b4 - Loop Offset Control, LS-bit.

Offset	B6	B5	B4
-3/4	1	1	1
-1/2	1	1	0
-1/4	1	0	1
0	X	0	0 (default)
+1/4	0	0	1
+1/2	0	1	0
+3/4	0	1	1

b3 - Freeze Data Control.
b2 - Coherent DPSK Enable Control:
Set to 0, default.
Set to 1, disables Q arm of dot product generator.
b1 - Loop Filter Input Control:
Set to 0, bit timming discriminator is connected to the loop filter (default).
Set to 1, FBI_{8-0} inputs are connected.
b0 - Input Data Format Control:
Set to 0, I_{s5-0} and Q_{s5-0} inputs are two's offset complement.
Set to 1, is offset binary format.

Q-Channel Convolutional Decoder:
Qualcomm Q1650 Read-Only registers. 32-bytes.

$2083 R BER Measurement LS-Byte Output Register.
$2084 R BER Measurement MS-Byte Output Register.

Q-Channel Convolutional Decoder: - Cont'd
Qualcomm Q1650 Write-Only registers. 32-bytes.

$2082 W Decoder Control Register #1.

b7..b5 - 0
b4 - Rate 1/3 Decoder: 1=ENABLE 0=INHIBIT
b3 - 0
b2 - Rate 1/2 decoder: 1=ENABLE 0=INHIBIT
b1 - 0
b0 - Input Mode: 1=SERIAL 0=PARALLEL

A8 - Bit-Sync & Viterbi Decoder Module - Cont'd

DDR R/W Function & Bit Pattern

$2083 W Decoder Control Register #2.
- b7..b5 - 0
- b4 - Differential Decoder Enable: 1=ENABLE 0=DISABLE
- b3 - Direct Data Mode: 1=BUS 0=PINS
- b2 - 0
- b1 - 0
- b0 - Decoder Input Mode: 1=SIGN_MAG 0=OFFSET_BINARY

$2084 W Decoder Control Register #3.
- b7..b3 - 0
- b2 - S/W Decoder Reset: 1=RESET 0=RUN
- b1 - 0
- b0 - ChainBack Path Depth: 1=96_STATES 0=48_STATES

$2088 W Normalization Test Bit Count Input Register.
(Determines the length of the synchronization monitor test)

$2089 W Normalization Test Normalize Count Input Register.
(Determines the normalization threshold level for the synchronization monitor test)

$208A W BER Period Input Register LS-Byte of 24-bit value.
$208B W BER Period Input Register CS-Byte
$208C W BER Period Input Register MS-Byte

$2095 W Reserved Register. Set to '0'. Must Write '0'
$2096 W Reserved Register. Set to '0'. Must Write '0'
$2097 W Normalization Test Value Enable Register.
Value is a Don't Care. Restarts the test.

$2098 W BER Test Value Enable Register.
Value is a Don't Care. Restarts the test.

A10 - Data Similator Module

ADDR R/W Function & Bit Pattern

$A000 R Module ID = $A (bits 4 thru 7)
- b7 - Wired to logic '1'
- b6 - Wired to logic '0'
- b5 - Wired to logic '1'
- b4..b0 - Wired to logic '0'

$A000 W I-ChTransmitter Data Control Register

- b7 - I-Ch Symbols G2: 1=INVERT 0=NORM
- b6 - Transmitter Data Source Select:
  - 0 - I-Ch Symbols
  - 1 - I-Ch Data
  - 2 - I-Ch Bi∅ Encoded
  - 3 - External Input: F/L User Commands
  - 4 - External Input: User Cmd Input + Shuttle F/L PN Code
- b3 - I-Ch Differential Encoder: 1=BYPASSED 0=ENABLED
- b2 - I-Ch Bi-Phase Converter: 1=ENABLED 0=BYPASSED
- b1..0 - Transponder I-Ch Data Output Select:
  - 0 - I-Ch Symbols
  - 1 - I-Ch Sim Data
  - 2 - I-Ch Sim Data Bi∅ Encoded

$A001 W Monitor Bus: Channel Select Register
- b7..6 - Scope Sync Select:
  - 0 - I-Channel Simulated Data Epoch
  - 1 - Q-Channel Simulated Data Epoch
  - 2 - I-Channel Simulated Data Clock
  - 3 - Q-Channel Simulated Data Clock
- b5..3 - Scope Channel-B Select:
  - 0 - I-Channel Simulated Data
  - 1 - Q-Channel Simulated Data
  - 2 - Q-Channel Simulated Data Clock
  - 3 - Shuttle PN Code Clock
  - 4 - I-Channel Bi∅ Data
  - 5 - Interleaver Output
- b2..0 - Scope Channel-A Select:
  - 0 - F/L User Commands
  - 1 - I-Channel Symbol Data
  - 2 - Q-Channel Symbol Data
  - 3 - I-Channel Simulated Data Clock
  - 4 - Shuttle PN Code
  - 5 - Q-Ch Bi∅ Data

A10 - Data Similator Module, Cond't

ADDR R/W Function & Bit Pattern

$A002 W Monitor Bus: Module Enable Register
- b7..3 - n/c
- b2 - Scope Sync: /ENA
- b1 - Scope Channel-B: /ENA
- b0 - Scope Channel-A: /ENA

$A003 W Q-Ch Transmitter Data control Register:
- b7 - Q-Ch NRZ Bi∅ Converter: 1=ENABLED 0=INHIBIT
- b6 - Q-Ch Differential Encoder: 1=INHIBIT 0=ENABLED
- b5 - Q-Ch Symbol G2: 1=INVERT 0=NORM
- b4 - Q-Ch Convolutional Encoder Rate: 1=RATE_1/3 0=RATE_1/2
- b3 - Q-Ch TLM Output: 1=ENABLED 0=INHIBIT
- b2..0 - Q-Ch Transmitter Data Source Select:
  - 0 - I-Ch Selected Data Source
  - 1 - Interleaver
  - 2 - Q-Ch Symbol Source
  - 3 - Q-Ch Data Source
  - 4 - Q-Ch Bi-∅ Data Source

$A004 W I/Q-Channel Telemetry Control Register
- b7 - n/c
- b6..5 - Q-Ch Bi-∅ Data Converter Format Select:
  - 0 - Bi∅-S
  - 1 - Bi∅-M
  - 2 - Differential Manchester
  - 3 - Bi∅-L
- b4 - Q-Ch Differential Encoder Output Select: 1=NRZ-S 0=NRZ-M
- b3 - n/c
- b2 - I-Ch NRZ Bi∅ Data Converter Output Select:
  - 0 - Bi∅-S
  - 1 - Bi∅-M
  - 2 - Differential Manchester
  - 3 - Bi∅-L
- b0 - I-Ch Differential Encoder Output Select: 1=NRZ-S 0=NRZ-M

A10 - Data Similator Module, Cond't

ADDR	R/W	Function & Bit Pattern
		I-Channel Simulated Data Clock Source (Qualcomm Q2334 Dual DDS), DDS #1:
$A100	W	Phase Increment A (PIRA) 1, bits 0-7 (LSB)
01	W	" " , bits 8-15
02	W	" " , bits 16-23
03	W	" " , bits 24-31 (MSB)
04	W	Phase Increment B (PIRB) 1, bits 0-7 (LSB)
05	W	" " , bits 8-15
06	W	" " , bits 16-23
07	W	" " , bits 24-31 (MSB)
08	W	Synchronous Mode Control (SMC) 1
09	W	Reserved
0A	W	Asynchronous Mode Control (AMC) 1
0B	W	Reserved
0C	W	Accumulator Reset (ARR) 1
0D	W	Reserved
0E	W	Asynchronous Hop Clock (AHC) 1
0F	W	Reserved
		Q-Channel Simulated Data Clock Source (Qualcomm Q2334 Dual DDS), DDS #2:
$A110	W	Phase Increment A (PIRA) 2, bits 0-7 (LSB)
11	W	" " , bits 8-15
12	W	" " , bits 16-23
13	W	" " , bits 24-31 (MSB)
14	W	Phase Increment B (PIRB) 2, bits 0-7 (LSB)
15	W	" " , bits 8-15
16	W	" " , bits 16-23
17	W	" " , bits 24-31 (MSB)
18	W	Synchronous Mode Control (SMC) 2
19	W	Reserved
1A	W	Asynchronous Mode Control (AMC) 2
1B	W	Reserved
1C	W	Accumulator Reset (ARR) 2
1D	W	Reserved
1E	W	Asynchronous Hop Clock (AHC) 2
1F	W	Reserved

A10 - Data Similator Module, Cond't

ADDR	R/W	Function & Bit Pattern
		I-Channel, Simulated Data Source, STEL-1032 PRN Coder #1
$A200	W	MASK Register bits 0-7
01	W	MASK Register bits 8-15
02	W	MASK Register bits 16-23
03	W	MASK Register bits 24-31 (MS-Byte)
04	W	INIT Register bits 0-7
05	W	INIT Register bits 8-15
06	W	INIT Register bits 16-23
07	W	INIT Register bits 24-31 (MS-Byte)
08	W	EPOCH Register bits 0-7
09	W	EPOCH Register bits 8-15
0A	W	EPOCH Register bits 16-23
0B	W	EPOCH Register bits 24-31 (MS-Byte)
0C	W	COUNT Register bits 0-7
0D	W	COUNT Register bits 8-15
0E	W	COUNT Register bits 16-23
0F	W	COUNT Register bits 24-31 (MS-Byte)
10	W	MUX Register bits 0-4
11	W	CTL Register bits 0-7
		Q-Channel, Simulated Data Source, STEL-1032 PRN Coder #2
$A220	W	MASK Register bits 0-7
21	W	MASK Register bits 8-15
22	W	MASK Register bits 16-23
23	W	MASK Register bits 24-31 (MS-Byte)
24	W	INIT Register bits 0-7
25	W	INIT Register bits 8-15
26	W	INIT Register bits 16-23
27	W	INIT Register bits 24-31 (MS-Byte)
28	W	EPOCH Register bits 0-7
29	W	EPOCH Register bits 8-15
2A	W	EPOCH Register bits 16-23
2B	W	EPOCH Register bits 24-31 (MS-Byte)
2C	W	COUNT Register bits 0-7
2D	W	COUNT Register bits 8-15
2E	W	COUNT Register bits 16-23
2F	W	COUNT Register bits 24-31 (MS-Byte)
30	W	MUX Register bits 0-4
31	W	CTL Register bits 0-7
$A300	W	PRN Load. (Data, don't care)

A12 - Ground Network Module

ADDR	R/W	Function & Bit Pattern
$C000	R	Module ID = $C (bits 4 thru 7) b7 - Wired to logic '1' b6 - Wired to logic '1' b5 - Wired to logic '0' b4 - Wired to logic '0' b3..b0 - Wired to logic '0'
$C000	W	Phase Mod Gain Control D/A Ch-1, SC Test Source, MS-Byte
$C001	W	Phase Mod Gain Control D/A Ch-1, SC Test Source, LS-Byte
$C002	W	Phase Mod Gain Control D/A Ch-2, Carrier Data Test Source, MS-Byte
$C003	W	Phase Mod Gain Control D/A Ch-2, Carrier Data Test Source, LS-Byte
$C004	W	Phase Mod Gain Control D/A Ch-3, User Cmd Subcarrier, MS-Byte
$C005	W	Phase Mod Gain Control D/A Ch-3, User Cmd Subcarrier, LS-Byte
$C006	W	Phase Mod Gain Control D/A Ch-4, Aux Input, MS-Byte
$C007	W	Phase Mod Gain Control D/A Ch-4, Aux Input, LS-Byte
$C008	W	Phase Mod Gain Control D/A, Update Ch-1 Reg, b7..b0 - "don't care"
$C009	W	Phase Mod Gain Control D/A, Update All Reg, b7..b0 - "don't care"
$C00A	W	Phase Mod Gain Control D/A, Update Ch-2 Reg, b7..b0 - "don't care"
$C00B	W	Phase Mod Gain Control D/A, Update All Reg, b7..b0 - "don't care"
$C00C	W	Phase Mod Gain Control D/A, Update Ch-3 Reg, b7..b0 - "don't care"
$C00D	W	Phase Mod Gain Control D/A, Update All Reg, b7..b0 - "don't care"
$C00E	W	Phase Mod Gain Control D/A, Update Ch-4 Reg, b7..b0 - "don't care"
$C00F	W	Phase Mod Gain Control D/A, Update All Reg, b7..b0 - "don't care"
$C010	W	Phase Modulator Data Source Select Register-A b7 - Aux. Phase Modulator Input: 1=ENA 0=INHIBIT b6 - User Command Subcarrier: 1=ENA 0=INHIBIT b5 - Carrier Data Test Source: 1=ENA 0=INHIBIT b4 - SubCarrier Test Source: 1=ENA 0=INHIBIT b3 - Sw LP Filter Control bit DN-800: 1=ENA 0=OUT b2 - Sw LP Filter Control bit DN-400: 1=ENA 0=OUT b1 - Sw LP Filter Control bit DN-200: 1=ENA 0=OUT b0 - Sw LP Filter Control bit DN-100: 1=ENA 0=OUT

A12 - Ground Network Module, Cont'd

ADDR R/W Function & Bit Pattern

$C020 W Phase Modulator Data Source Select Register-B

b7 - Sw LP Filter Control bit DN-80: 1=ENA 0=OUT
b6 - Sw LP Filter Control bit DN-40: 1=ENA 0=OUT
b5 - Sw LP Filter Control bit DN-20: 1=ENA 0=OUT
b4 - Sw LP Filter Control bit DN-10: 1=ENA 0=OUT
b3 - Sw LP Filter Control bit DN-8: 1=ENA 0=OUT
b2 - Sw LP Filter Control bit DN-4: 1=ENA 0=OUT
b1 - Sw LP Filter Control bit DN-2: 1=ENA 0=OUT
b0 - Sw LP Filter Control bit DN-1: 1=ENA 0=OUT

Switchable Low Pass Filter (Datel FLJ-D2) logic coding table:

Fc	SLPF Control bit to be Enabled
100 Hz	DN-1
200 Hz	DN-2
400 Hz	DN-4
800 Hz	DN-8
1 KHz	DN-10
2 KHz	DN-20
4 KHz	DN-40
8 KHz	DN-80
10 KHz	DN-100
20 KHz	DN-200
40 KHz	DN-400
80 Khz	DN-800
90 KHz	DN-800, DN-100
100 KHz	DN-800, DN-200
120 KHz	DN-800, DN-400
140 KHz	DN-800, DN-400, DN-200
150 KHz	DN-800, DN-400, DN-200, DN-100
159.9KHz	DN-800, DN-400, DN-200, DN-100, DN-80

$C030 W Subcarrier Data Level Control, 8-bit Control Word, CW = int[(20 - Greq(dB))/0.375]

A12 - Ground Network Module

ADDR R/W Function & Bit Pattern

DSP_Bus

(Spare NCO) (Qualcomm Q2334 Dual DDS), DDS #1:

$60	W	Phase Increment A (PIRA) 1, bits 0-7 (LSB)
61	W	" " , bits 8-15
62	W	" " , bits 16-23
63	W	" " , bits 24-31 (MSB)
64	W	Phase Increment B (PIRB) 1, bits 0-7 (LSB)
65	W	" " , bits 8-15
66	W	" " , bits 16-23
67	W	" " , bits 24-31 (MSB)
68	W	Synchronous Mode Control (SMC) 1 b7..4 - xxx b3 - Hop Clock PM Mod Enable (HPME) b2 - External Mux Enable (EME) b1 - External PM Mod Enable (EPME) b0 - xxx
69	W	Reserved
6A	W	Asynchronous Mode Control (AMC) 1 b7..6 - xxx b5 - PM Register Add Enable (PMAE) b4 - xxx b3 - Output Format: 0=2's compl, 1=offset binary b2..0 - D/A converter Size: set to 0x06, 12 bits
6B	W	Reserved
6C	W	Accumulator Reset (ARR) 1
6D	W	Reserved
6E	W	Asynchronous Hop Clock (AHC) 1
6F	W	Reserved

Rx Carrier Freq Source (Qualcomm Q2334 Dual DDS), DDS #2:

$70	W	Phase Increment A (PIRA) 2, bits 0-7 (LSB)
71	W	" " , bits 8-15
72	W	" " , bits 16-23
73	W	" " , bits 24-31 (MSB)
74	W	Phase Increment B (PIRB) 2, bits 0-7 (LSB)
75	W	" " , bits 8-15
76	W	" " , bits 16-23
77	W	" " , bits 24-31 (MSB)
78	W	Synchronous Mode Control (SMC) 2
79	W	Reserved
7A	W	Asynchronous Mode Control (AMC) 2
7B	W	Reserved
7C	W	Accumulator Reset (ARR) 2
7D	W	Reserved
7E	W	Asynchronous Hop Clock (AHC) 2
7F	W	Reserved

RF Distribution Unit (RFDU) Memory Map

ADDR	R/W	Function & Bit Pattern	
$0000	R	Transmit Output Level Range Attenuator Sense b7 - n/c b6 - n/c b5 - n/c b4 - Tx Atn Status: ERR/OK b3 - Tx Atn 40 dB: OUT/IN b2 - TX Atn 40 dB: OUT/IN b1 - TX Atn 20 dB: OUT/IN b0 - TX Atn 10 dB: OUT/IN	RC50
$0001	R	Receiver Input Level Range Attenuator Sense b7 - n/c b6 - n/c b5 - n/c b4 - n/c b4 - Rx Atn Status: ERR/OK b2 - Rx Atn 40 dB: OUT/IN b1 - Rx Atn 20 dB: OUT/IN b0 - Rx Atn 10 dB: OUT/IN	RC51
$0002	R	Transfer Switch Sense b7 - n/c b6 - XFER-Switch Status: ERR/OK b5 - S6 - SPA Source: IF/S-BAND b4 - S5 -SPA IF Source: EXT/370IF b3 - S4 - SPA S-Band Source: TX / RX b2 - S3 - RX Input: J3-RX_IN /DIPLEXER b1 - S2 - TX Outout: DIPLEXER/J2-TX_OUT b0 - S1 -TS Source: XLATOR/ ANT	RC52
$0003	R	Signal Monitors: b7 - +15 Volt Power Supply Monitor: OK/ERR b6 - +24 Volt Power Supply Monitor: OK/ERR b5 - n/c b4 - n/c b3 - A4 Rx x16-Multiplier: OK/ERR b2 - A3 Tx x14-Multiplier: OK/ERR b1 - A2 QPSK Modulator: OK/ERR b0 - A1 X3-Multiplier & Linear Modulator: OK/ERR	RC53
$0004	R	GPIB Address Switch b7..4 - Address: 0 thru 15 (0 .. F: Hex values) b3..0 - not used	RC54

RF Distribution Unit (RFDU) Memory Map,Cont'd

ADDR	R/W	Function & Bit Pattern	
$0000	W	Transmit Output Level Range Attenuator Control	WC50
		b7 - n/c [GRTS Only: MA Cal Attenuator, 16 dB: IN/OUT, Pin-6]	
		b6 - n/c [GRTS Only: MA Cal Attenuator, 8 dB: IN/OUT, Pin-5]	
		b5 - n/c [GRTS Only: MA Cal Attenuator, 4 dB: IN/OUT, Pin-4]	
		b4 - n/c [GRTS Only: MA Cal Attenuator, 2 dB: IN/OUT, Pin-3]	
		b3 - Tx Atn 40 dB: IN/OUT [GRTS Only: MA Cal Atten, 1 dB: IN/OUT, Pin-2]	
		b2 - TX Atn 40 dB: IN/OUT [GRTS Only: MA Cal Atten, 0.5 dB: IN/OUT, Pin-1]	
		b1 - TX Atn 20 dB: IN/OUT	
		b0 - TX Atn 10 dB: IN/OUT	
$0001	W	Receiver Input Level Range Attenuator Control	WC51
		b7 - n/c	
		b6 - n/c	
		b5 - n/c	
		b4 - n/c	
		b3 - n/c	
		b2 - Rx Atn 40 dB: IN/OUT	
		b1 - Rx Atn 20 dB: IN/OUT	
		b0 - Rx Atn 10 dB: IN/OUT	
$0002	W	Transfer Switch Control	WC52
		b7 - n/c	
		b6 - n/c	
		b5 - S6 - SPA Source: IF/ S-BAND	
		b4 - S5 -SPA IF Source: EXT/370IF	
		b3 - S4 - SPA S-Band Source: TX / RX	
		b2 - S3 - RX Input: J3-RX_IN/ DIPLEXER	
		b1 - S2 - TX Outout: DIPLEXER/J2-TX_OUT	
		b0 - S1 -TS Source: XLATOR/ ANT	
$0003	W	Transmit Output Level Fine Attenuator	WC53
		b7 - TX RF Output: ON/OFF	
		b6 - 32 dB Attenuator Section: 1=IN 0=OUT	
		b5 - 16 dB Attenuator Section: 1=IN 0=OUT	
		b4 - 8 dB Attenuator Section: 1=IN 0=OUT	
		b3 - 4 dB Attenuator Section: 1=IN 0=OUT	
		b2 - 2 dB Attenuator Section: 1=IN 0=OUT	
		b1 - 1 dB Attenuator Section: 1=IN 0=OUT	
		b0 - 0.5 dB Attenuator Section: 1=IN 0=OUT (Not Used)	
$0004	W	I-Channel QPSK Modulator Control	WC54
		B7 - n/c	
		b6 - n/c	
		b5 - n/c	
		b4 - PSK Mode select: QPSK/BPSK	
		b3 - 8 dB Attenuator section: 1=OUT 0=IN	
		b2 - 4 dB Attenuator Section: 1=OUT 0=IN	
		b1 - 2 dB Attenuator Section: 1=OUT 0=IN	
		b0 - 1 dB Attenuator section: 1=OUT 0=IN	

RF Distribution Unit (RFDU) Memory Map, Cont'd

ADDR	R/W	Function & Bit Pattern	
$0005	W	Q-Channel QPSK Modulator Control B7 - n/c b6 - n/c b5 - n/c b4 - Linear PM Modulator: IN/OUT b3 - 8 dB Attenuator section: 1=IN 0=OUT b2 - 4 dB Attenuator Section: 1=IN 0=OUT b1 - 2 dB Attenuator Section: 1=IN 0=OUT b0 - 1 dB Attenuator section: 1=IN 0=OUT	WC55
$0006	W	Transmit Output Leveler D/A: Byte value: 0 thru 255 will output a voltage ranging from 0 to 10 VDC resulting in the TX output level ranging from +5 dBm to +15dBm.	WC56
$0007	-	Not used!	